



Integrated Device Technology, Inc.

# CMOS STATIC RAM 1 MEG (128K x 8-BIT)

IDT71024

## FEATURES:

- 128K x 8 advanced high-speed CMOS static RAM
- Commercial (0° to 70°C), Industrial (-40° to 85°C) and Military (-55° to 125°C) temperature options
- Equal access and cycle times
  - Military: 15/17/20/25ns
  - Industrial: 15/20ns
  - Commercial: 12/15/17/20ns
- Two Chip Selects plus one Output Enable pin
- Bidirectional inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Available in 300 and 400 mil Plastic SOJ, and LCC packages
- Military product compliant to MIL-STD-883, Class B

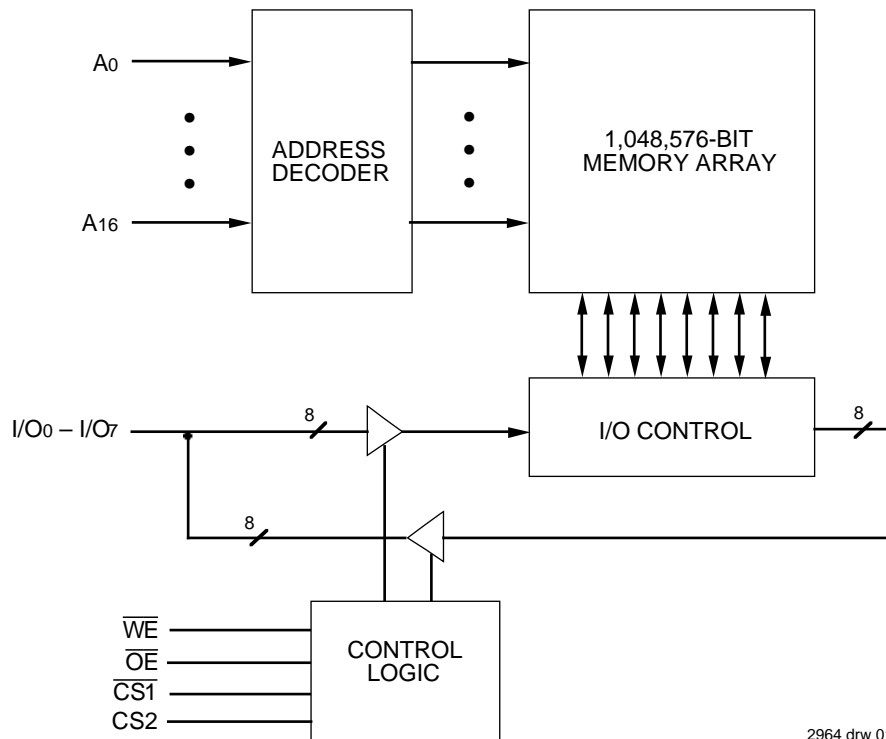
## DESCRIPTION:

The IDT71024 is a 1,048,576-bit high-speed static RAM organized as 128K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

The IDT71024 has an output enable pin which operates as fast as 6ns, with address access times as fast as 12ns available. All bidirectional inputs and outputs of the IDT71024 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used; no clocks or refreshes are required for operation.

The IDT71024 is packaged in 32-pin 300 mil Plastic SOJ, 32-pin 400 mil Plastic SOJ, and 32-pin 400 x 820 mil LCC packages.

## FUNCTIONAL BLOCK DIAGRAM



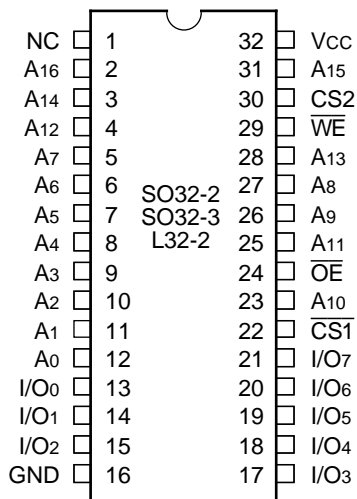
2964 drw 01

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**MILITARY, INDUSTRIAL AND COMMERCIAL TEMPERATURE RANGES**

**MAY 1997**

## PIN CONFIGURATION



2964 drw 02

### SOJ/LCC TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Rating	Com'l, Ind'l	Mil.	Unit
VTERM <sup>(2)</sup>	Terminal Voltage Relative to GND	-0.5 to +7.0	-0.5 to +7.0	V
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	1.25	1.25	W
IOUT	DC Output Current	50	50	mA

### NOTES:

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- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- VTERM must not exceed Vcc + 0.5V.

## TRUTH TABLE<sup>(1,2)</sup>

INPUTS				I/O	FUNCTION
WE	CS1	CS2	OE		
X	H	X	X	High-Z	Deselected-Standby (ISB)
X	VHC <sup>(3)</sup>	X	X	High-Z	Deselected-Standby (ISB1)
X	X	L	X	High-Z	Deselected-Standby (ISB)
X	X	VLC <sup>(3)</sup>	X	High-Z	Deselected-Standby (ISB1)
H	L	H	H	High-Z	Outputs Disabled
H	L	H	L	DATAOUT	Read Data
L	L	H	X	DATAIN	Write Data

### NOTES:

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- H = VIH, L = VIL, X = Don't care.
- VLC = 0.2V, VHC = Vcc - 0.2V.
- Other inputs ≥ VHC or ≤ VLC.

## RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 0.5V
Industrial	-40°C to +85°C	0V	5.0V ± 0.5V
Military	-55°C to +125°C	0V	5.0V ± 0.5V

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## RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	Vcc+0.5	V
VIL	Input Low Voltage	-0.5 <sup>(1)</sup>	—	0.8	V

### NOTE:

2964 tbl 04

- VIL (min.) = -1.5V for pulse width less than 10ns, once per cycle.

## DC ELECTRICAL CHARACTERISTICS

Vcc = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71024		Unit
			Min.	Max.	
ILI	Input Leakage Current	Vcc = Max., VIN = GND to Vcc	—	5	μA
ILO	Output Leakage Current	Vcc = Max., CS1 = VIH, CS2 = VIL, VOUT = GND to Vcc	—	5	μA
VOL	Output LOW Voltage	IOL = 8mA, Vcc = Min.	—	0.4	V
VOH	Output HIGH Voltage	IOH = -4mA, Vcc = Min.	2.4	—	V

2964 tbl 05

## DC ELECTRICAL CHARACTERISTICS<sup>(1)</sup>

( $V_{CC} = 5.0V \pm 10\%$ ,  $V_{LC} = 0.2V$ ,  $V_{HC} = V_{CC} - 0.2V$ )

Symbol	Parameter	71024S12		71024S15		71024S17		71024S20		71024S25		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I <sub>CC</sub>	Dynamic Operating Current, $CS2 \geq V_{IH}$ and $CS2 \geq V_{IH}$ and $\overline{CS1} \leq V_{IL}$ , Outputs Open, $V_{CC} = \text{Max.}$ , $f = f_{MAX}^{(2)}$	160	—	155	180	150	170	140	160	—	145	mA
I <sub>SB</sub>	Standby Power Supply Current (TTL Level) $CS1 \geq V_{IH}$ or $CS2 \leq V_{IL}$ , Outputs Open, $V_{CC} = \text{Max.}$ , $f = f_{MAX}^{(2)}$	35	—	35	40	35	40	35	40	—	35	mA
I <sub>SB1</sub>	Full Standby Power Supply Current (CMOS Level) $CS1 \geq V_{HC}$ , or $CS2 \leq V_{LC}$ Outputs Open, $V_{CC} = \text{Max.}$ , $f = 0^{(2)}$ , $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$	10	—	10	15	10	15	10	15	—	15	mA

### NOTES:

- All values are maximum guaranteed values.
- $f_{MAX} = 1/t_{RC}$  (all address inputs are cycling at  $f_{MAX}$ );  $f = 0$  means no address input lines are changing.

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## DC ELECTRICAL CHARACTERISTICS<sup>(1)</sup>

( $V_{CC} = 5.0V \pm 10\%$ ,  $V_{LC} = 0.2V$ ,  $V_{HC} = V_{CC} - 0.2V$ )

Symbol	Parameter	71024S15	71024S20	Unit
		Industrial	Industrial	
I <sub>CC</sub>	Dynamic Operating Current, $CS2 \geq V_{IH}$ and $CS2 \geq V_{IH}$ and $\overline{CS1} \leq V_{IL}$ , Outputs Open, $V_{CC} = \text{Max.}$ , $f = f_{MAX}^{(2)}$	180	160	mA
I <sub>SB</sub>	Standby Power Supply Current (TTL Level) $CS1 \geq V_{IH}$ or $CS2 \leq V_{IL}$ , Outputs Open, $V_{CC} = \text{Max.}$ , $f = f_{MAX}^{(2)}$	45	45	mA
I <sub>SB1</sub>	Full Standby Power Supply Current (CMOS Level) $CS1 \geq V_{HC}$ , or $CS2 \leq V_{LC}$ Outputs Open, $V_{CC} = \text{Max.}$ , $f = 0^{(2)}$ , $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$	15	15	mA

### NOTES:

- All values are maximum guaranteed values.
- $f_{MAX} = 1/t_{RC}$  (all address inputs are cycling at  $f_{MAX}$ );  $f = 0$  means no address input lines are changing.

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## CAPACITANCE

( $T_A = +25^\circ\text{C}$ ,  $f = 1.0\text{MHz}$ , SOJ package)

Symbol	Parameter <sup>(1)</sup>	Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	$V_{IN} = 3dV$	7	pF
C <sub>I/O</sub>	I/O Capacitance	$V_{OUT} = 3dV$	8	pF

### NOTE:

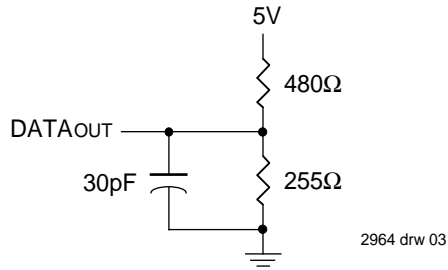
- This parameter is guaranteed by device characterization, but is not production tested.

2964 tbl 08

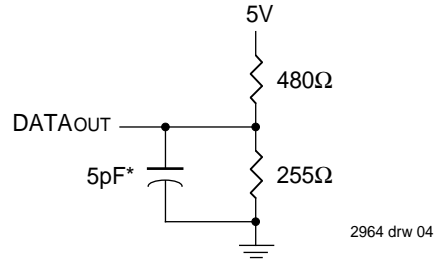
**AC TEST CONDITIONS**

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2964 tbl 09



**Figure 1. AC Test Load**



\*Including jig and scope capacitance.

**Figure 2. AC Test Load  
 (for tCLZ, tOLZ, tCHZ, tOHZ, tOW, and tWHZ)**

**AC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5.0V \pm 10\%$ , All Temperature Ranges)

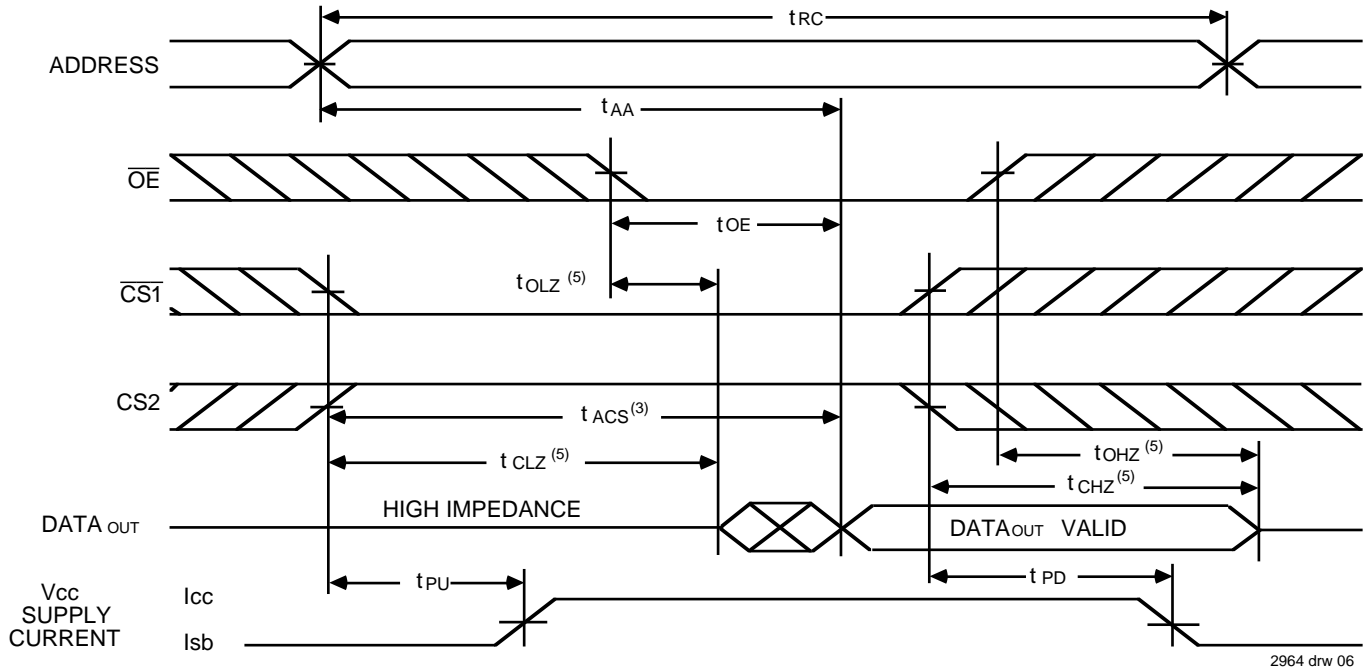
Symbol	Parameter	71024S12 <sup>(1)</sup>		71024S15		71024S17 <sup>(3)</sup>		71024S20		71024S25 <sup>(2)</sup>		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>												
t <sub>RC</sub>	Read Cycle Time	12	—	15	—	17	—	20	—	25	—	ns
t <sub>AA</sub>	Address Access Time	—	12	—	15	—	17	—	20	—	25	ns
t <sub>ACS</sub>	Chip Select Access Time	—	12	—	15	—	17	—	20	—	25	ns
t <sub>CLZ</sub> <sup>(4)</sup>	Chip Select to Output in Low-Z	3	—	3	—	3	—	3	—	3	—	ns
t <sub>CHZ</sub> <sup>(4)</sup>	Chip Deselect to Output in High-Z	0	6	0	7	0	8	0	8	0	10	ns
t <sub>OE</sub>	Output Enable to Output Valid	—	6	—	7	—	8	—	8	—	10	ns
t <sub>OLZ</sub> <sup>(4)</sup>	Output Enable to Output in Low-Z	0	—	0	—	0	—	0	—	0	—	ns
t <sub>OHZ</sub> <sup>(4)</sup>	Output Disable to Output in High-Z	0	5	0	5	0	6	0	7	0	10	ns
t <sub>OH</sub>	Output Hold from Address Change	4	—	4	—	4	—	4	—	4	—	ns
t <sub>PU</sub> <sup>(4)</sup>	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	0	—	ns
t <sub>PD</sub> <sup>(4)</sup>	Chip Deselect to Power-Down Time	—	12	—	15	—	17	—	20	—	25	ns
<b>Write Cycle</b>												
t <sub>WC</sub>	Write Cycle Time	12	—	15	—	17	—	20	—	25	—	ns
t <sub>AW</sub>	Address Valid to End-of-Write	10	—	12	—	13	—	15	—	15	—	ns
t <sub>CW</sub>	Chip Select to End-of-Write	10	—	12	—	13	—	15	—	15	—	ns
t <sub>AS</sub>	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
t <sub>WP</sub>	Write Pulse Width	10	—	12	—	13	—	15	—	15	—	ns
t <sub>WR</sub>	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t <sub>DW</sub>	Data Valid to End-of-Write	7	—	8	—	9	—	9	—	10	—	ns
t <sub>DH</sub>	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
t <sub>OW</sub> <sup>(4)</sup>	Output Active from End-of-Write	3	—	3	—	3	—	4	—	4	—	ns
t <sub>WHZ</sub> <sup>(4)</sup>	Write Enable to Output in High-Z	0	5	0	5	0	7	0	8	0	9	ns

**NOTES:**

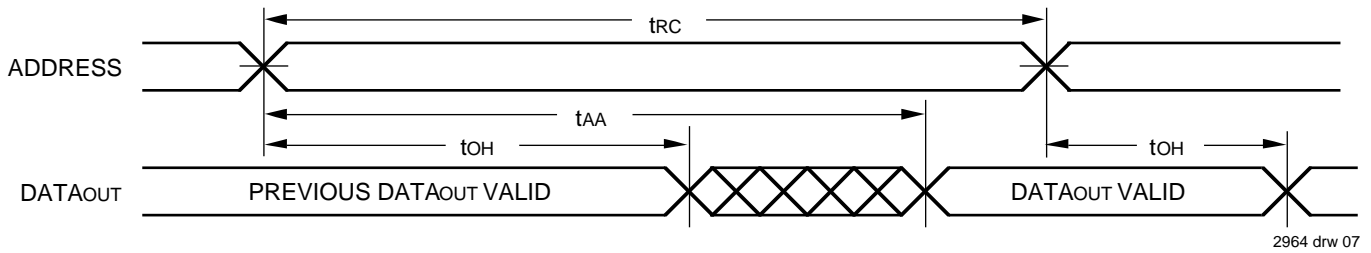
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. 0°C to +70°C and -55°C to +125°C temperature ranges only.
4. This parameter guaranteed with the AC load (Figure 2) by device characterization, but is not production tested.

2964 tbl 010

**TIMING WAVEFORM OF READ CYCLE NO. 1<sup>(1)</sup>**



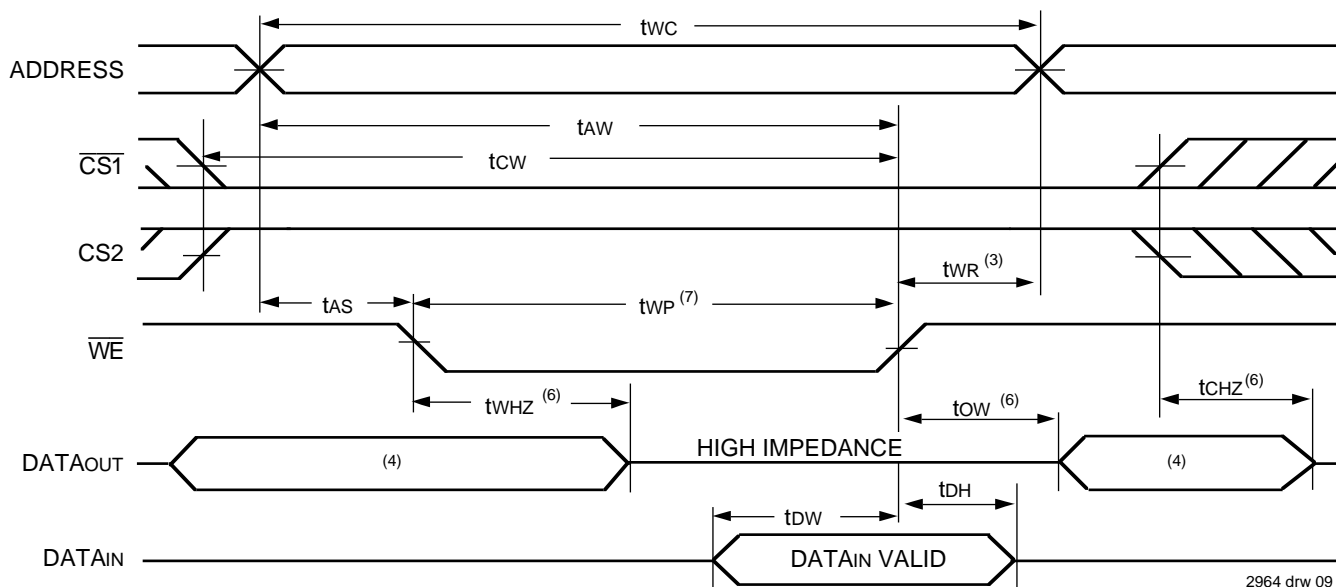
**TIMING WAVEFORM OF READ CYCLE NO. 2<sup>(1, 2, 4)</sup>**



**NOTES:**

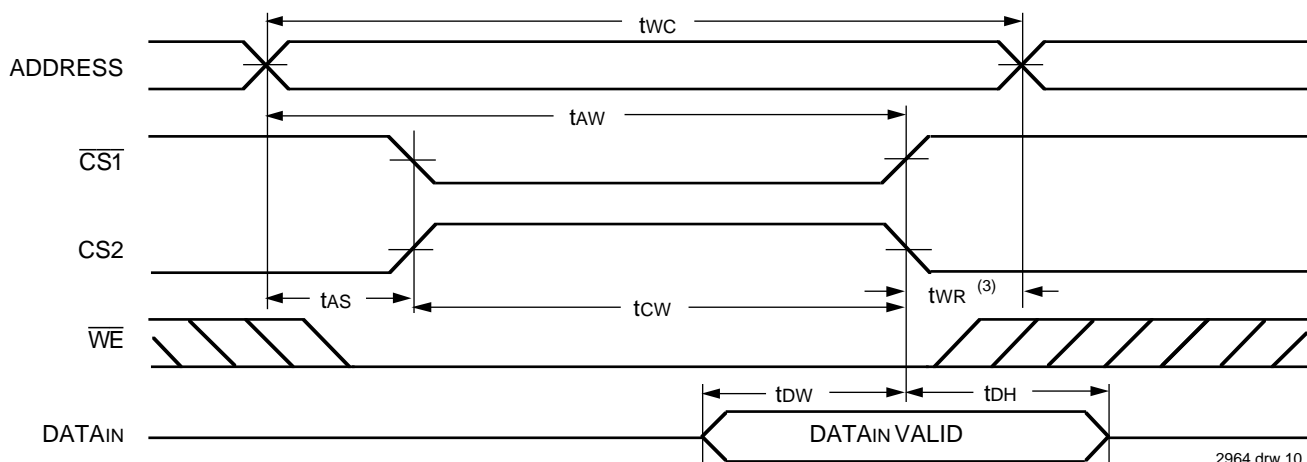
1.  $\overline{WE}$  is HIGH for Read Cycle.
2. Device is continuously selected,  $\overline{CS1}$  is LOW,  $\overline{CS2}$  is HIGH.
3. Address must be valid prior to or coincident with the later of  $\overline{CS1}$  transition LOW and  $\overline{CS2}$  transition HIGH; otherwise  $t_{AA}$  is the limiting parameter.
4.  $\overline{OE}$  is LOW.
5. Transition is measured  $\pm 200\text{mV}$  from steady state.

**TIMING WAVEFORM OF WRITE CYCLE NO. 1 ( $\overline{WE}$  CONTROLLED TIMING)<sup>(1, 2, 5, 7)</sup>**



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**TIMING WAVEFORM OF WRITE CYCLE NO. 2 ( $\overline{CS1}$  AND CS2 CONTROLLED TIMING)<sup>(1, 2, 5)</sup>**

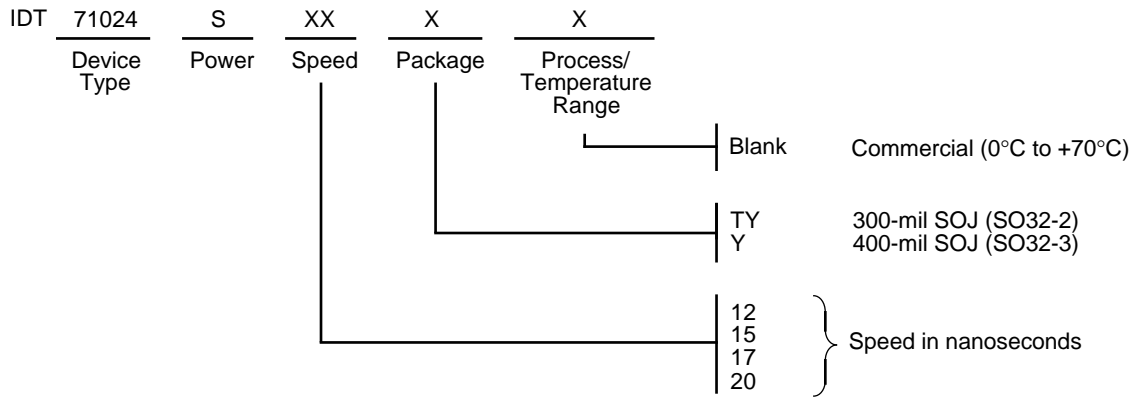


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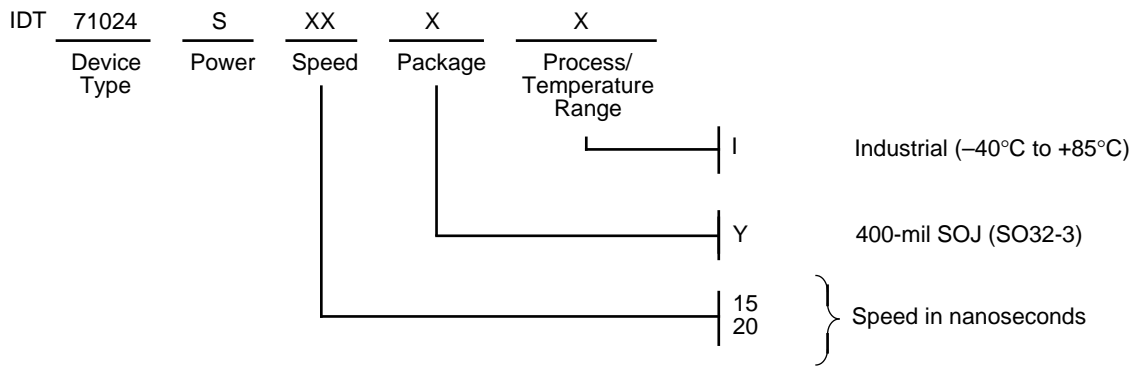
**NOTES:**

1.  $\overline{WE}$  must be HIGH,  $\overline{CS1}$  must be HIGH, or CS2 must be LOW during all address transitions.
2. A write occurs during the overlap of a LOW  $\overline{CS1}$ , HIGH CS2, and a LOW  $\overline{WE}$ .
3. tWR is measured from the earlier of either  $\overline{CS1}$  or  $\overline{WE}$  going HIGH or CS2 going LOW to the end of the write cycle.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the  $\overline{CS1}$  LOW transition or the CS2 HIGH transition occurs simultaneously with or after the  $\overline{WE}$  LOW transition, the outputs remain in a high impedance state.  $\overline{CS1}$  and CS2 must both be active during the tcw write period.
6. Transition is measured  $\pm 200\text{mV}$  from steady state.
7.  $\overline{OE}$  is continuously HIGH. During a  $\overline{WE}$  controlled write cycle with  $\overline{OE}$  LOW, tWP must be greater than or equal to tWHZ + tDW to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If  $\overline{OE}$  is HIGH during a  $\overline{WE}$  controlled write cycle, this requirement does not apply and the minimum write pulse is the specified tWP.

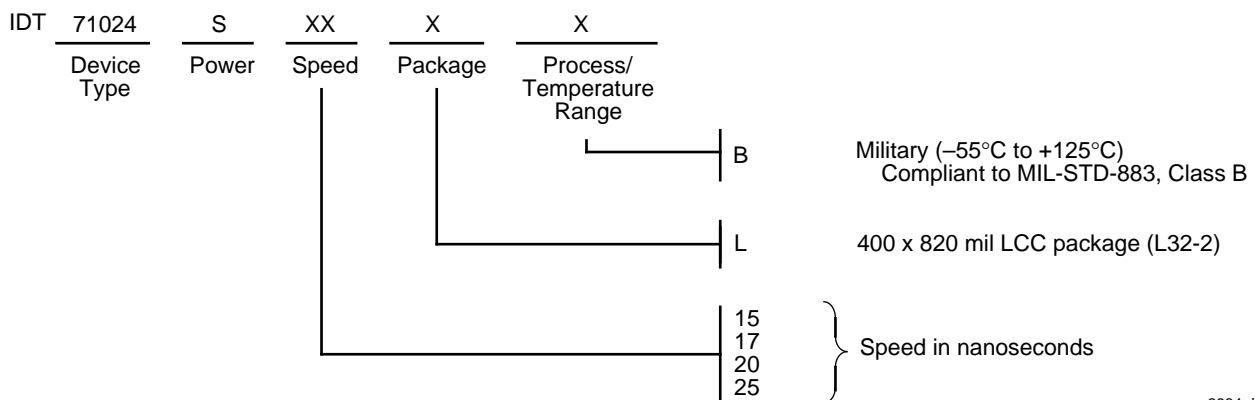
**ORDERING INFORMATION**



2964 drw 11



2964 drw 12



2964 drw 13